



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/760,741	01/17/2001	Jerry M. Brooks	M4065.0374/P374	5786

24998 7590 05/21/2004

DICKSTEIN SHAPIRO MORIN & OSHINSKY LLP
2101 L STREET NW
WASHINGTON, DC 20037-1526

EXAMINER

CHU, CHRIS C

ART UNIT	PAPER NUMBER
----------	--------------

2815

DATE MAILED: 05/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Applicati n N .

09/760,741

Applicant(s)

BROOKS, JERRY M.

Examiner

Chris C. Chu

Art Unit

2815

-- The MAILING DATE of this c mmunicati n appears n the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 February 2004.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1, 4 - 9, 11 - 21 and 32 - 42 is/are pending in the application.
- 4a) Of the above claim(s) 32 - 39 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 4 - 9, 11 - 21, 41 and 42 is/are rejected.
- 7) ☒ Claim(s) 41 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filed on October 15, 2003 has been received and entered in the case.

Claim Objections

2. Claim 12 is objected to under 37 CFR 1.75(c), as being of improper dependent form for failing to correct further change the number of a previous cancelled claim to non-cancelled claim. Applicant is required to cancel the claim, or amend the claim to place the claim in proper dependent form, or rewrite the claim in independent form. Such as, in line 1, "claim 10" should be --claim 1--.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 1, 4 – 9 and 11 – 14 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

Art Unit: 2815

In claim 1, line 8, the specification fails to describe the term "solely" in the limitation "said at least one semiconductor die being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material". Since the final product of this invention clearly shows in Fig. 7 an encapsulating material and the flowable adhesive material are used to secure the bottom surface of the semiconductor die to the top surface of the support structure, hence the new added term "solely" in the claim 1 is not supported by the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claim 14 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 14, it is unclear what the applicant regards as "said encapsulating material fills in at least some portion of a space between said bottom surface of said die and said top surface of said support structure". That is, the limitation of claim 1 "solely by a flowable adhesive material," precludes the encapsulating material filling the space between the die and the support structure. Therefore, the limitation is contradicting each other, hence the claim cannot be understood.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 6, 7, 12 – 14 and 42 are rejected under 35 U.S.C. 102(b) as being anticipated by Cognetti et al. '752.

Regarding claim 1, Cognetti et al. discloses in e.g., Fig. 1, Fig. 2, column 2, lines 53 - 56 and column 2, line 64 – column 3, line 4 a semiconductor assembly comprising:

- a support structure (10) having a top surface; and
- at least one semiconductor die (20) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die (20) being secured at its bottom surface to said top surface of said support structure solely by a flowable adhesive material (16) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die, said top surface of said support structure having at least one electrical contact area (12) at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication (22) with said at least one electrical contact area.

Regarding claim 6, Cognetti et al. discloses in e.g., Fig. 1, Fig. 2, column 2, lines 53 - 56 and column 2, line 64 – column 3, line 4 said flowable adhesive material (16)

Art Unit: 2815

covering an area less than or equal to "about" 90% of said at least one semiconductor die bottom surface area.

Regarding claim 7, Cognetti et al. discloses in e.g., Fig. 1, Fig. 2, column 2, lines 53 - 56 and column 2, line 64 – column 3, line 4 said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die bottom surface area.

Regarding claim 12, (for examination purposes, examiner assumed the claim 12 is a dependent claim of the claim 1) Cognetti et al. discloses in e.g., Fig. 1, Fig. 2, column 2, lines 53 - 56 and column 2, line 64 – column 3, line 4 said at least one electrical contact area being a bonding pad (12).

Regarding claim 13, Cognetti et al. discloses in e.g., Fig. 1, Fig. 2, column 2, lines 53 - 56 and column 2, line 64 – column 3, line 4 an encapsulating material (the injection molded resin that encapsulates the die) encapsulating said die, electrical communication (the element 22) and at least a portion of said support structure (the portion right under the element 20).

Regarding claim 14, Cognetti et al. discloses in e.g., Fig. 2 and column 2, lines 29 – 33 said encapsulating material fills (the injection molded resin locates between the die and the top surface of to support structure) in at least some portion of a space between said bottom surface of said die and said top surface of said support structure.

Regarding claim 42, Cognetti et al. discloses in e.g., Fig. 1, Fig. 2, column 2, lines 53 - 56 and column 2, line 64 – column 3, line 4 a semiconductor assembly comprising:

- a support structure (10) having a top surface; and

Art Unit: 2815

- at least one semiconductor die (20) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said at least one semiconductor die (20) being secured at its bottom surface to said top surface of said support structure by a flowable adhesive material (16) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die, said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die's bottom surface area, said top surface of said support structure having at least one electrical contact area (12) at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication (22) with said at least one electrical contact area.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 8 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cognetti et al. in view of McMahon '712.

Regarding claims 8 and 9, Cognetti et al. discloses the claimed invention except for a distance between an electrical contact area and said perimeter of said at least one

Art Unit: 2815

semiconductor die is less than or equal to about 200 microns. Since McMahon shows in Fig. 5A an electrical contact area (254, at the right-side) extends under the perimeter of a semiconductor die (202), McMahon teaches the following limitation a “distance between an electrical contact area and a perimeter of at least one semiconductor die being less than or equal to *about* 200 microns”. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Cognetti et al. by using the distance being less than or equal to about 200 microns as taught by McMahon. The ordinary artisan would have been motivated to modify Cognetti et al. in the manner described above for at least the purpose of diminishing circuit feature sizes and more power for the semiconductor device (column 1, lines 37 - 48).

11. Claims 15 - 17 and 19 - 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura in view of McMahon '712.

Regarding claims 8, 9 and 15, Matsumura discloses in e.g., Fig. 1, Fig. 13 and column 6, line 67 – column 7, line 4 a semiconductor assembly comprising:

- a first semiconductor die (1) having a top and a bottom surface;
- a second semiconductor die (7) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said first semiconductor die (1), said second die (7) being secured at its bottom surface to said top surface of said first semiconductor die by a flowable adhesive material (5) which does not extend past any one of the sides of said perimeter of said second semiconductor die; and

Art Unit: 2815

- wherein the top surface of said first semiconductor die has at least one electrical contact area (3) positioned at a location exterior to said perimeter of said second semiconductor die.

Matsumura discloses the claimed invention except for a distance between an electrical contact area and said perimeter of said at least one semiconductor die is less than or equal to about 428 microns. Since McMahon shows in Fig. 5A an electrical contact area (254, at the right-side) extends under the perimeter of a semiconductor die (202), McMahon teaches the following limitation a “distance between an electrical contact area and a perimeter of at least one semiconductor die being less than or equal to *about* 428 microns”. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsumura by using the distance being less than or equal to about 428 microns as taught by McMahon. The ordinary artisan would have been motivated to modify Matsumura in the manner described above for at least the purpose of diminishing circuit feature sizes and more power for the semiconductor device (column 1, lines 37 - 48).

Regarding claim 16, Matsumura discloses in e.g., Fig. 1 said first semiconductor die (1) being secured to a support structure (17).

Regarding claim 17, Matsumura discloses in e.g., Fig. 1 said support structure (17) being a film.

Regarding claim 19, Matsumura discloses in e.g., column 6, line 67 – column 7, line 4 an adhesive material being an epoxy.

Art Unit: 2815

Regarding claim 20, Matsumura discloses in e.g., Fig. 1 said flowable adhesive material (5) covering an area less than or equal to "about" 90% of said at least one semiconductor die bottom surface area.

Regarding claim 21, Matsumura discloses in e.g., Fig. 1 said flowable adhesive material covering an area greater than or equal to "about" 50% of said at least one semiconductor die bottom surface area.

12. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Matsumura in view of McMahon as applied to claims 15 and 16 above, and further in view of Crowley et al. '147.

Matsumura, as modified, discloses the claimed invention except for the support structure being a printed circuit board. However, Crowley et al. teaches in Fig. 1 and column 3, line 65 – column 4, line 4 a support structure (16) being a printed circuit board. Thus, it would have been obvious to one of ordinary skill in the art at the time when the invention was made to modify Matsumura by using the printed circuit board for the support structure as taught by Crowley et al. The ordinary artisan would have been motivated to modify Matsumura in the manner described above for at least the purpose of decreasing a thermal expansion between the chip and the support structure.

13. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schueller et al. '530. in view of Takiar et al. '435.

Regarding claim 40, Schueller et al. discloses in e.g., Fig. 1 a semiconductor assembly comprising:

Art Unit: 2815

- a support structure (14) having a top surface; and
- a first semiconductor die (20) having a perimeter, including four sides, and a top and bottom surface, said bottom surface having a smaller area than said top surface of said support structure, said first semiconductor die (20) being secured at its bottom surface to said top surface of said support structure by a compressed adhesive material (24) which does not extend past any one of the sides of said perimeter of said at least one semiconductor die such that there is a first cavity along at least a portion of said perimeter between said support structure and said first semiconductor die, said first cavity being filled with an encapsulating material (26) such that only said adhesive material and said encapsulating material are between said first semiconductor die and said support structure, said top surface of said support structure having at least one electrical contact area (at the area where the wire 22 is connected) at a distance outside said perimeter of said at least one semiconductor die, said at least one semiconductor die being in electrical communication (22) with said at least one electrical contact area.

While Schueller et al. teaches the use of the adhesive material, Schueller et al. does not appear to provide any example of the adhesive's specific composition. Takiar et al. teaches in e.g., Fig. 5, Fig. 10 and column 5, line 51 the adhesive material (48) may be composed of a flowable adhesive material (e.g., epoxy). It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the epoxy as the specific material to form the adhesive material between the die and the

Art Unit: 2815

supporting structure of Schueller et al. as taught by Takiar et al. to reduce the thermal shock between the support structure and the die.

Furthermore, Schueller et al. teaches that the compressed adhesive material (24) does not extend past two sides (the left and right sides) of the perimeter of the at least one semiconductor die (20). However, Schueller et al. does not appear to provide any example of the adhesive's cover area that does not extend past the other two sides of the perimeter of the semiconductor die. It would have been obvious to one of ordinary skill in the art at the time when the invention was made to apply the flowable adhesive material at the specific location under the semiconductor die to form the flowable adhesive material does not extend past the other two sides of the perimeter of the semiconductor die as taught by Schueller et al.'s left and right sides of the semiconductor die to reduce the amount of the adhesive material that increases the speed of process by decreasing the time to cure the adhesive.

Allowable Subject Matter

14. Claim 41 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 41 contains allowable subject matter because none of the references of record teach or suggest, either singularly or in combination, at least the limitation of a second semiconductor die having a perimeter, including four sides, and a top and bottom surface, the second semiconductor die being secured at its bottom surface to the top surface of a first semiconductor die by a compressed flowable adhesive material which

Art Unit: 2815

does not extend past any one of the sides of the perimeter of the second semiconductor die such that there is a second cavity along at least a portion of the perimeter between the first semiconductor die and the second semiconductor die, the second cavity being filled with an encapsulating material.

Response to Arguments

15. Applicant's arguments with respect to claims 1, 40 and 42 have been considered but are moot in view of the new ground(s) of rejection.

However, for the claim 15, the Applicant's arguments filed February 25, 2004 have been fully considered but they are not persuasive.

On page 21, paragraph two, applicant argues "even if McMahon's Fig. 5A shows the bond pad within the perimeter of the chip, such a showing fails to teach or suggest these limitations. As also noted above, McMahon is silent about the distance of the bond pad from the perimeter of the chip where McMahon shows the bond pad outside the chip perimeter." This argument is not persuasive. First, the rejected claim 15, lines 5 - 13 clearly defines the perimeter of the second chip including four sides and the first semiconductor die has at least one electrical contact area positioned at a location exterior to said perimeter of the second semiconductor chip.

Second, the contact area (254, at the right-side) of McMahon is located exterior to one of the perimeter (e.g., the perimeter of the right-side surface) of the chip and the contact area (254) is located within one of the perimeter (e.g., the perimeter of the left-side surface) of the chip. Thus, McMahon teaches the following limitation a "distance

Art Unit: 2815

between said electrical contact area and said perimeter of said second semiconductor die is less than or equal to *about* 428 microns”.

For the above reason, the rejection is maintained.

Conclusion

16. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Nakajima et al. discloses an adhesive and a cap between the chip and the support structure.

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Art Unit: 2815

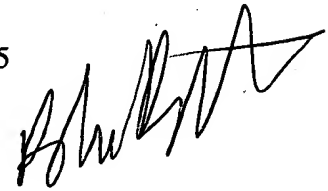
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chris C. Chu whose telephone number is 571-272-1724.

The examiner can normally be reached on 11:30 - 8:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 517-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chris C. Chu
Examiner
Art Unit 2815



c.c.
5/12/04 6:43:57 PM

**BRADLEY BAUMEISTER
PRIMARY EXAMINER**